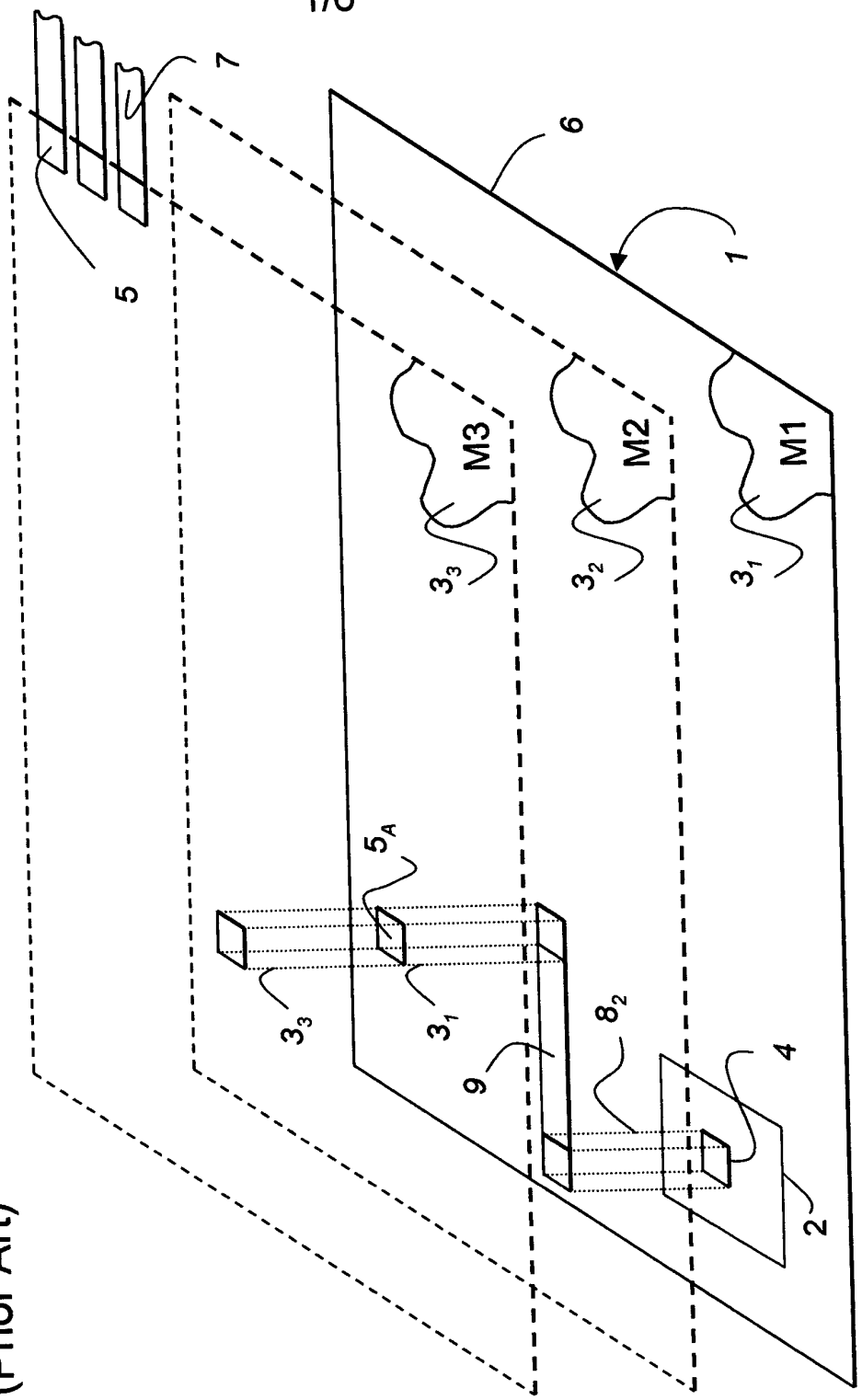

Fig. 1
(Prior Art)

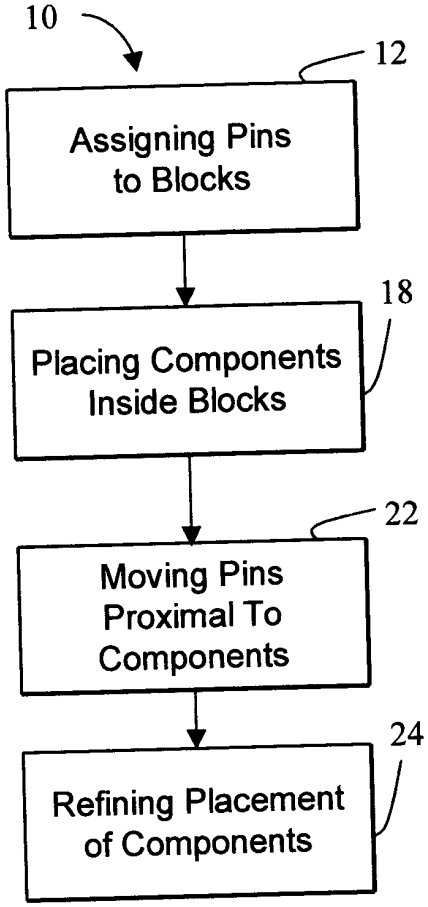

Fig. 2

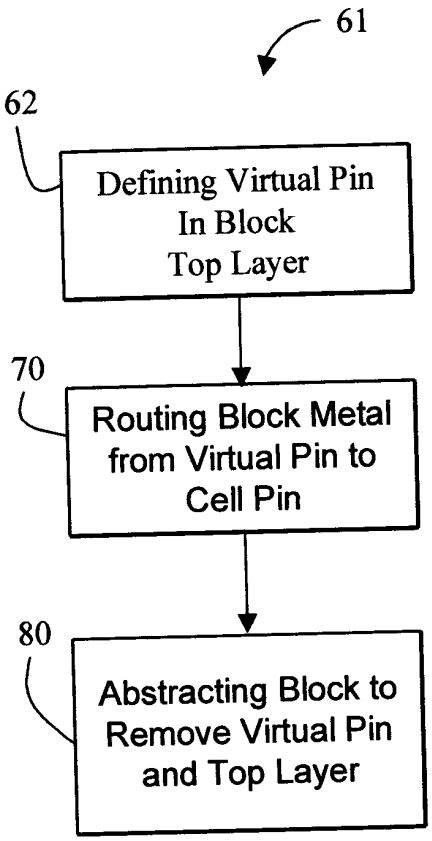
61
62
Defining Virtual Pin In Block Top Layer
70
Routing Block Metal from Virtual Pin to Cell Pin
80
Abstracting Block to Remove Virtual Pin and Top Layer

Fig. 8

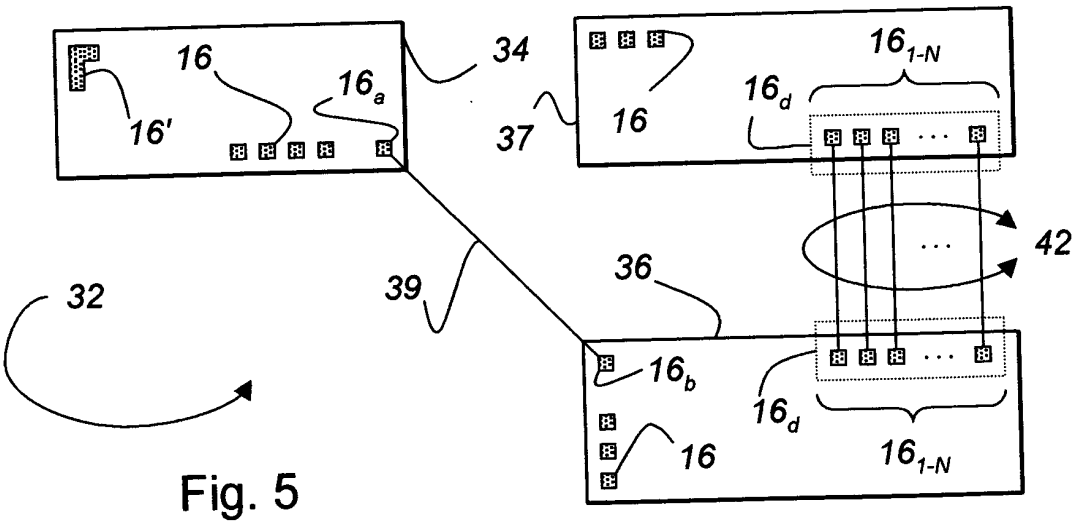

Fig. 5

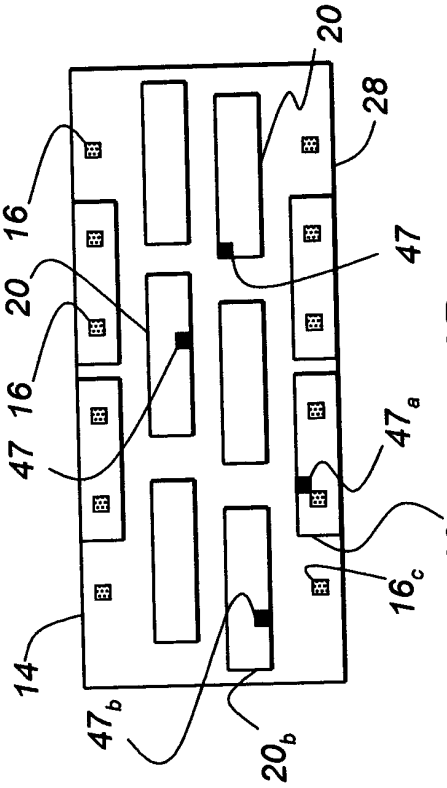

Fig. 3B

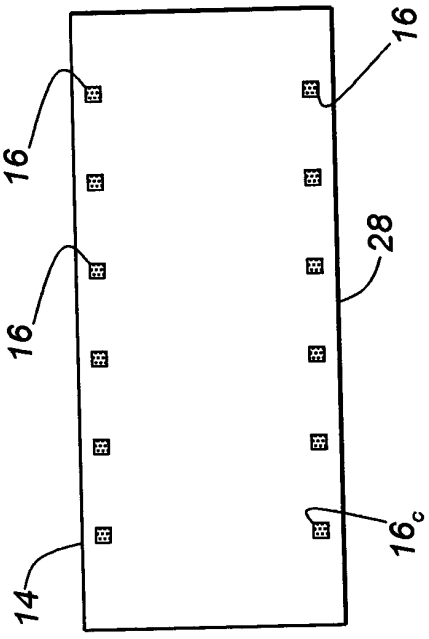

Fig. 3A

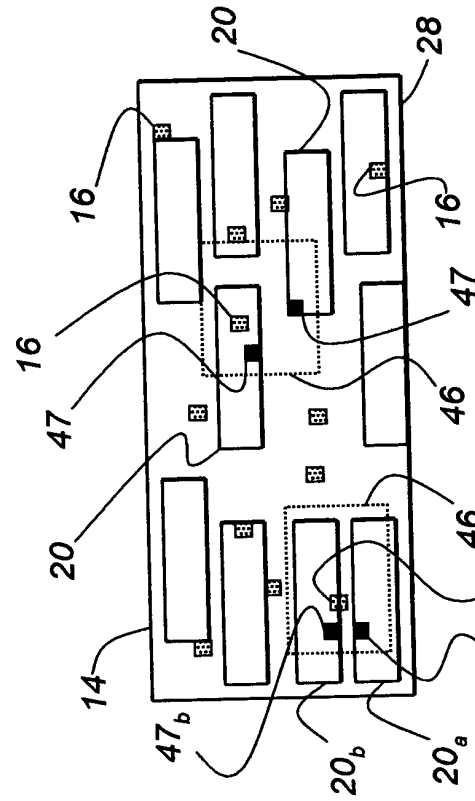

Fig. 3D

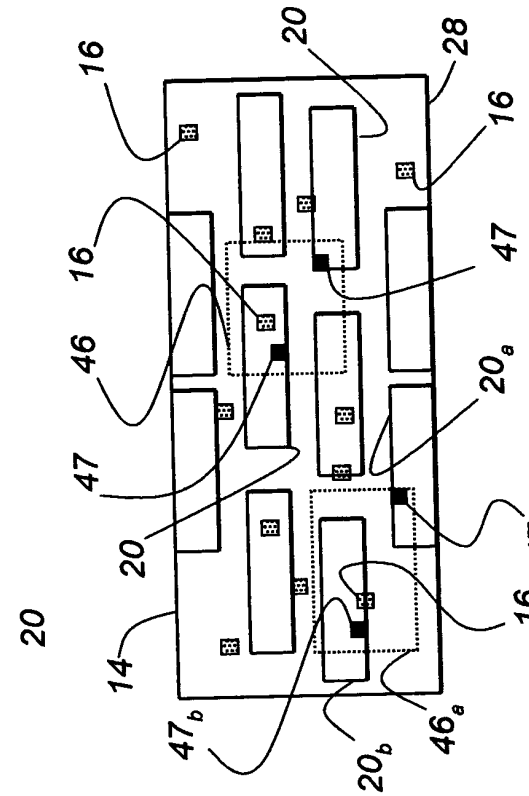

Fig. 3C

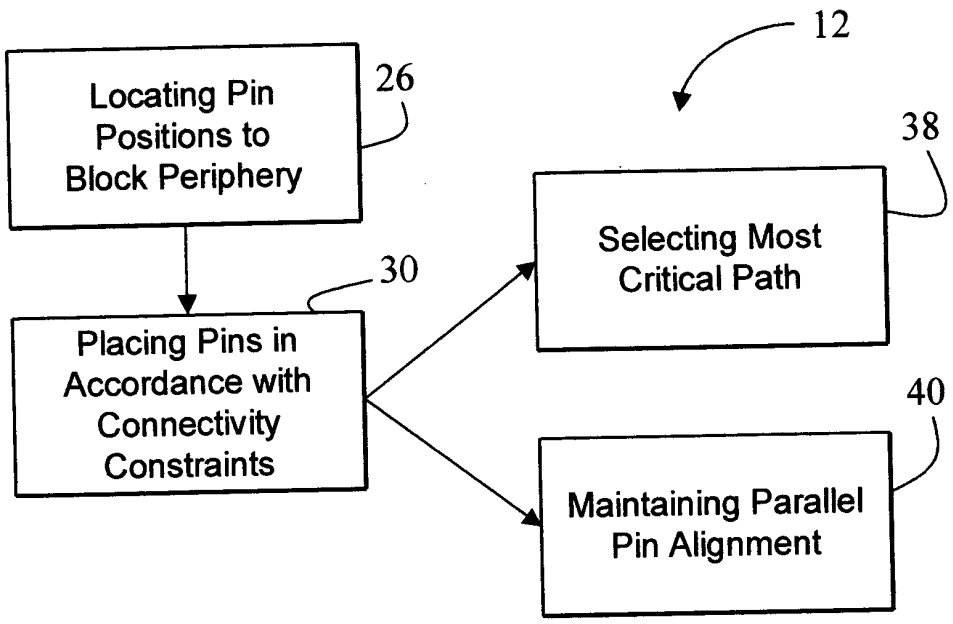
12
Locating Pin Positions to Block Periphery
26
38
Selecting Most Critical Path
30
Placing Pins in Accordance with Connectivity Constraints
40
Maintaining Parallel Pin Alignment

Fig. 4

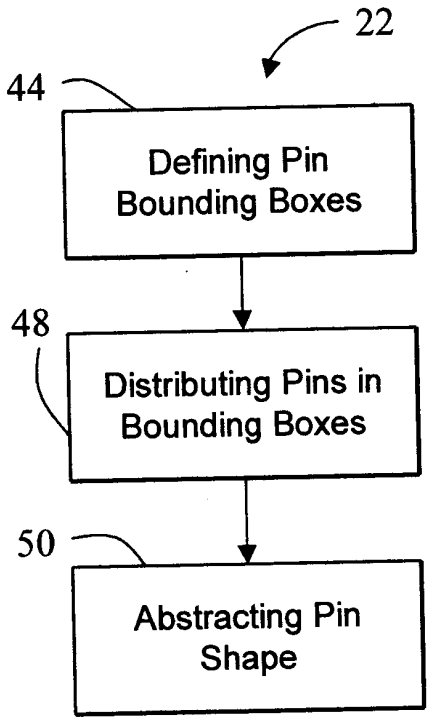
22
44
Defining Pin Bounding Boxes
48
Distributing Pins in Bounding Boxes
50
Abstracting Pin Shape

Fig. 6

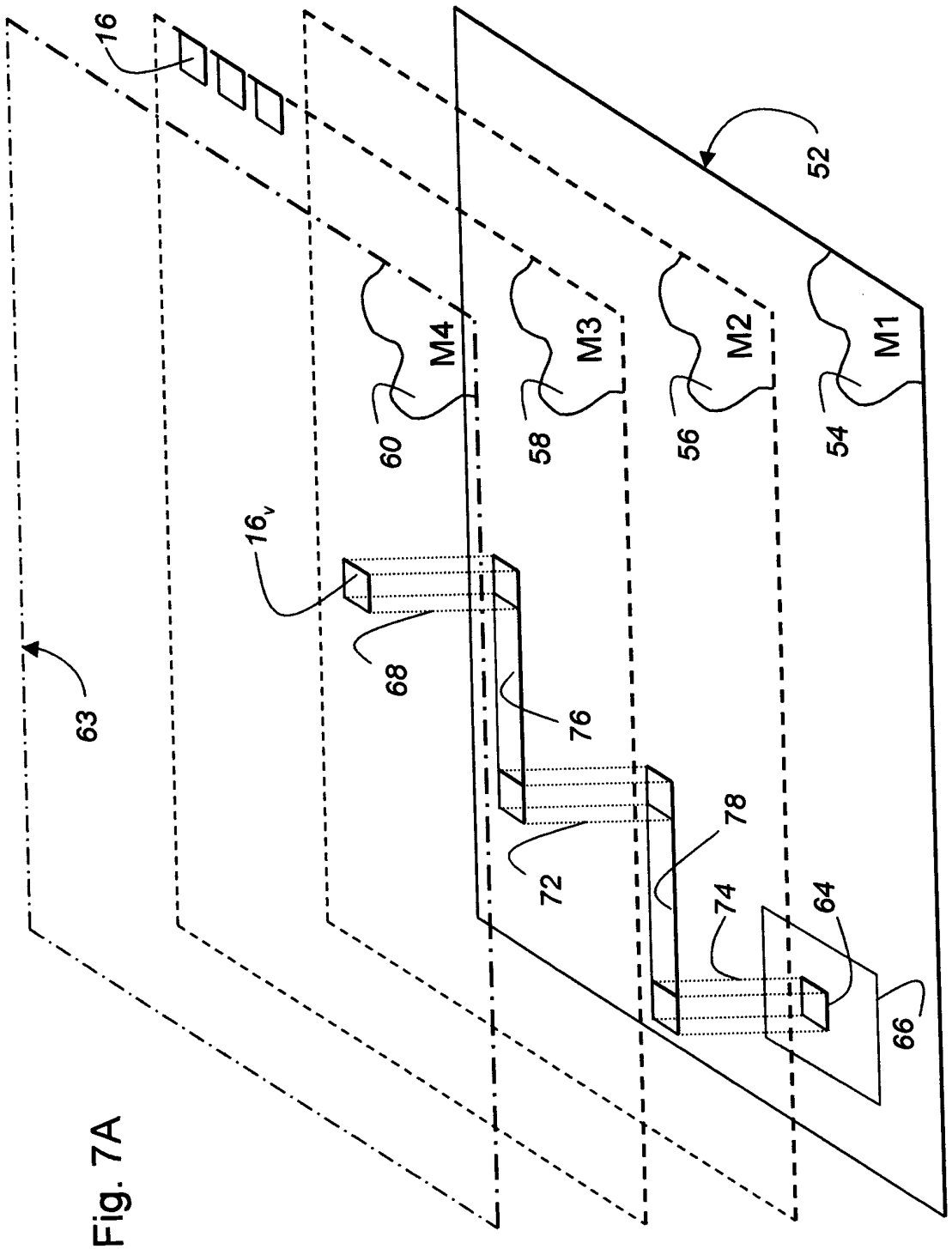

Fig. 7A

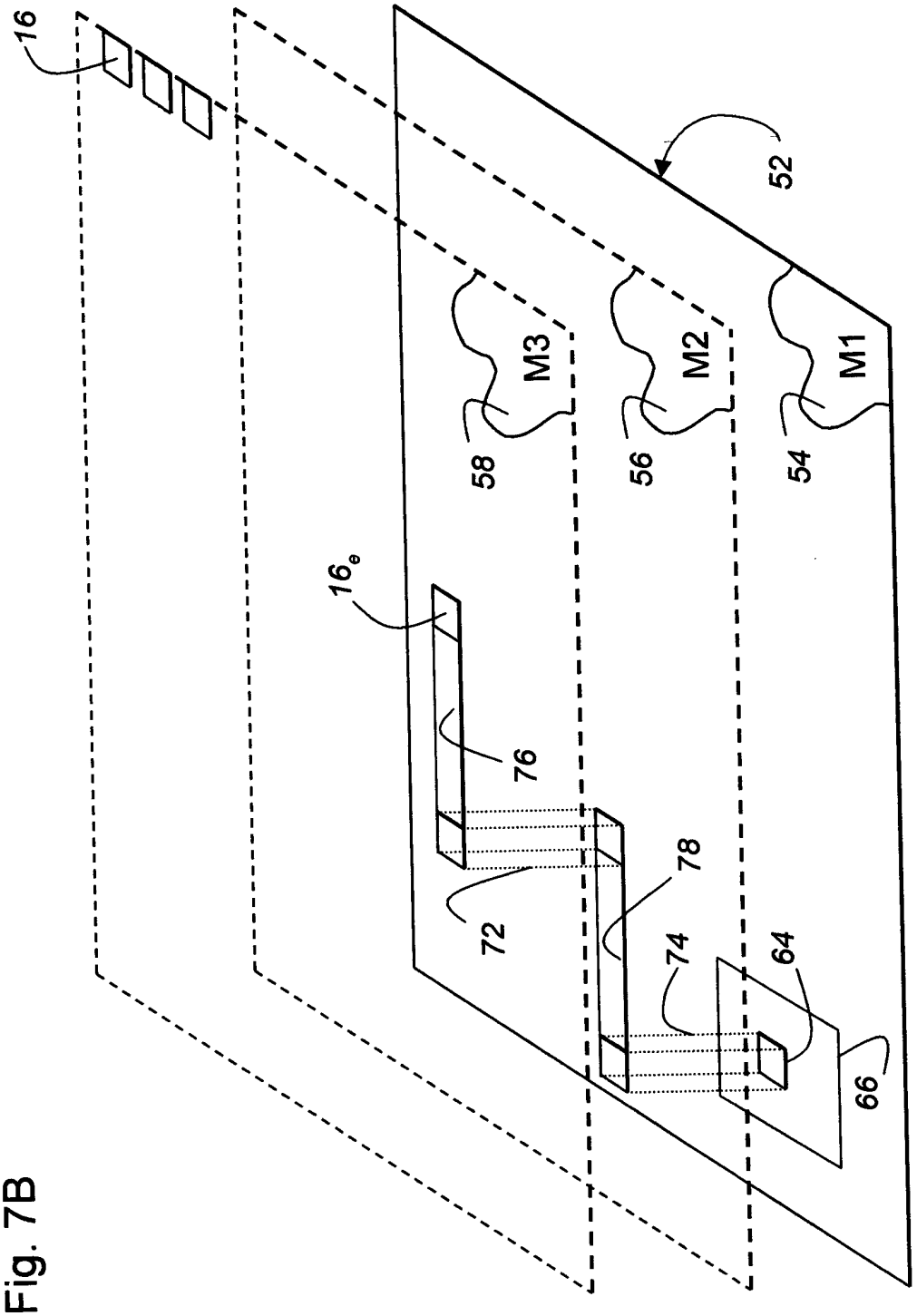

Fig. 7B